FERNANDO GARCÍA REDONDO

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SUMMARY

Over 12 years of hands on experience on electronic systems research, focusing on HW aware algorithm optimization –TinyML HW, Computing-in-memory architectures and algorithms design for constrained devices; modeling and simulation of emerging devices.

PROFESSIONAL EXPERIENCE

Arm Research, Arm Ltd.

2022 - Present Staff Research Engineer
2018 - 2022 Senior Research Engineer

- HW aware algorithm optimization. Design of ultra low power MoNo MCU, a 10uW active 10nW sleep Cortex M33 running real-time KWS using 16KB of RAM.
- HW/SW Co-design for analog Compute In Memory systems based on non-volatile crossbars within MNEMOSENE project.
- Stochastic analysis and numerical modeling of MTJ structures for MRAM memories. Compact model and circuitry design for reliable MRAM.
- Design and implementation of AMS platform for the modeling and simulation of Intermittent Compute (IC) Systems within Triffid project.
- Design of Triffid Energy-Harvesting power control and testbed platform –including Gen2 RFID reader SDK development, RF agents, PCB and lab-equipment orchestration.
- IP Generation and dissemination.

Universidad P. C. ICAI

2017 Associate Lecturer
Associate Lecturer in Integrated Circuit Design. Course coordinator.

Universidad Politécnica de Madrid

2017 Postdoctoral Researcher
Design and simulation of RRAM-CMOS based circuit applications

2012-2017 Ph.D. Candidate

- Characterization of physical resistive switching devices, RRAMs.
- Compact modeling and simulation of resistive switching devices.
- RRAM-CMOS circuit design focusing on reliability and low power operation.

2010-2013 Research Grant
RTL design and implementation of radar and communication systems.

EDUCATION

Universidad Politécnica de Madrid

2017 Ph.D. in Electronic Systems Engineering
Resistive RAM: Simulation and Modeling for Reliable Design
2012 MSc. in Electronic Systems Engineering
2011 BSc + MSc (ABET accredited) in Telecommunication Engineering

SELECTED RESEARCH DISSEMINATION AND IP GENERATION

2021 AnalogNets: ML-HW Co-Design of Noise-robust TinyML Models and Always-On Analog Compute-in-Memory Accelerator
2021 A Fokker-Planck Solver to Model MTJ Stochasticity
2021 –17 dBm Differential charge pump EPC Gen2 UHF RFID demodulator for 9 dB receive sensitivity boost
2020 Training DNN IoT Applications for Deployment On Analog NVM Crossbars
2020 27.2 MoNo: A performance-regulated 0.8-to-38MHz DVFS ARM cortex-M33 SIMD MCU with 10nW sleep power
2019 Applications of computation-in-memory architectures based on memristive devices
2016 SPICE compact modeling of bipolar/unipolar memristor switching governed by electrical thresholds

Patents Arm has filed 24 patent applications on which I am a named inventor, addressing CiM ML accelerators, low power systems, IC systems and NVM memories.

HONORS & AWARDS

2019 Extraordinary Doctorate Awards, Universidad Politécnica de Madrid
2012 Degree with Honors, Final Degree Project, BSc.