Fernando García-Redondo

PhD & Electronic Systems Engineer

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"Drive projects and learn to solve problems in the field of circuits and systems for AI and ML"

Education

- *Universidad Politécnica de Madrid* — *Madrid, Spain*
  PhD. in Electronic Systems Engineering — *June 2017*
- *Universidad Politécnica de Madrid* — *Madrid, Spain*
  MSc in Electronic Systems Engineering — *2012*
- *Universidad Politécnica de Madrid* — *Madrid, Spain*
  BSc + MSc (ABET accredited) in Telecommunication Engineering — *2011*

Skills

Machine Learning & Hardware	Design of ML algorithms for constrained HW: μ-controllers and computation-in-memory
Electronic Systems Design	HW & SW Co-design: RRAM/CMOS Hybrid Designs + FPGAs + μ-controllers + SW: SPICE/Spectre circuit simulators, Verilog-A, VHDL
ML Technologies	TensorFlow, TensorflowLite, CMSIS-NN
Programming Languages	C++, Python, C, Java, Matlab
Other & Methodologies	STL, Boost, Design Patterns, Git
Languages	English, Spanish

Experience

- *Arm Research Department, Arm Ltd* — *Cambridge, UK*
  Senior Research Engineer — *March 2018 - Now*
- *Integrated Systems Laboratory, Universidad Politécnica de Madrid* — *Madrid, Spain*
  RRAM/CMOS PostDoc Researcher — *June 2017 - February 2018*
- *Escuela Técnica Superior de Ingeniería ICAI, Universidad Pontificia Comillas* — *Madrid, Spain*
  VLSI Design Lecturer and Course Coordinator — *Jan. 2017 - June 2017*
- *Integrated Systems Laboratory, Universidad Politécnica de Madrid* — *Madrid, Spain*
  RRAM/CMOS Circuits Researcher and Digital Electronics Engineer — *Oct. 2013 - June 2017*
- *Integrated Systems Laboratory, Universidad Politécnica de Madrid* — *Madrid, Spain*
  Electronics Research Grant — *Jan. 2010 - Oct. 2013*
- *Nexus5, Software Company* — *Madrid, Spain*
  Software Engineer — *Sept. 2006 - Dec. 2009*

Research Areas

- *Design of analog/digital acelerators for ML*
- *Study of ML algorithms for constrained hardware*
- *Memristor/RRAM modeling and simulation*
- *Design and development of automated CAD tools for the use of memristors in circuits*

Research Stays

- *Universidad Autónoma de Barcelona, UAB* — *Barcelona, Spain*
  Unipolar OxRAM characterization (reliability) — *July 2015*
- *Nanotechnology Research Group, ECS, University of Southampton* — *Southampton, UK*
  Bipolar CBRAM characterization and compact modeling — *Feb.-May 2015.*
- *Universidad de las Islas Baleares, UIB* — *Mallorca, Spain*
  SRAM Under Radiation Research — *September 2014*

Organization of International Congress

- *Publications Chair* — *Lausanne, Switzerland*
  16th IEEE International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD 2019) — *2019*
- *Publications Chair* — *Prague, Czech Republic*
  15th IEEE International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD 2018) — *2018*

Reviewer Activity

- *Neural Computing and Applications, Springer*
- *Microelectronics Journal, Elsevier*
- *Journal on Emerging and Selected Topics in Circuits and Systems, IEEE*
- *Transactions on Nanotechnology, IEEE*
- *Transactions on Emerging Topics in Computing, IEEE*
- *Transactions on Electron Devices, IEEE*
- *Transactions on Circuits and Systems I: Regular Papers. IEEE*

Teaching Activity

- *Escuela Técnica Superior de Ingeniería ICAI, Universidad Pontificia Comillas* — *Madrid, Spain*
  Associate Professor, MsC: "Integrated Circuits Design" — *2017*
- *Universidad Politécnica de Madrid* — *Madrid, Spain*
  Teaching collaborator, Msc: "Radar, Technologies, Equipment and System Design" — *2015*
- *Universidad Politécnica de Madrid* — *Madrid, Spain*
  Teaching collaborator, "Digital Electronics" — *2015*
- *Universidad Politécnica de Madrid* — *Madrid, Spain*
  Teaching collaborator, "Electronic Circuits" — *2015*
- *Universidad Politécnica de Madrid* — *Madrid, Spain*
  Teaching collaborator, "Micro-Electronics Laboratory" — *2014*
- *DotNetClub IEEE, Madrid* — *Madrid, Spain*
  Seminar, "Client/Server applications using .Net" — *2007*

Courses and Seminars

- *SSR, Universidad Politécnica de Madrid* — *Madrid, Spain*
  Introducing Deep Learning and TensorFlow — *2017*
- *University of Texas* — *MOOC Online*
  Embedded Systems- Shape the World — *2016*
- *Stanford University* — *MOOC Online*
  Machine Learning — *2015*
- *Cadence* — *MOOC Online*
  SKILL Development of Parameterized Cells vIC6.1.5 (ILS) — *2014*
- *Cadence* — *MOOC Online*
  C++ Language Fundamentals for Design and Verification v12.2 (ILS) — *2014*
- *Cadence* — *MOOC Online*
  SKILL Language Programming vIC 6.1.5 Cadence — *2014*
- *Cadence* — *MOOC Online*
  Introduction - SKILL Language Programming vIC 6.1.5 Cadence — *2013*

Publications

Journals

2018 **Self-controlled multilevel writing architecture for fast training in neuromorphic RRAM applications**, Fernando García-Redondo, Marisa López-Vallejo, *Nanotechnology, Volume 29, Issue 40, Pages 405203. DOI: https://doi.org/10.1088/1361-6528/aad2fa*

2017 **Auto-Erasable RRAM Architecture Secured Against Physical and Firmware Attacks**, Fernando García-Redondo, Marisa López-Vallejo, *IEEE Transactions on Circuits and Systems I: Regular Papers. Volume 5, Issue 5, Pages 1581 - 1590. DOI: 10.1109/TCSI.2017.2755123*

2017 **On the Design and Analysis of Reliable RRAM-CMOS Hybrid Circuits**, Fernando García-Redondo, Marisa López-Vallejo, *IEEE Transactions on Nanotechnology . Volume: 16, Issue:3, Pages 514-522. July 2017. DOI: 10.1109/TNANO.2017.2697311*

2017 **Reconfigurable Writing Architecture for Reliable RRAM Operation in Wide Temperature Ranges**, Fernando García-Redondo, Pablo Royer, Marisa López-Vallejo, Hernán Aparicio, Pablo Ituero, Carlos A. López-Barrio, *IEEE Transactions on Very Large Scale Integration (VLSI) Systems. Volume: 25, Issue: 4, Pages 1224 - 1235. April 2017. DOI: 10.1109/TVLSI.2016.2634083*

2016 **SPICE Compact Modeling of Bipolar/Unipolar Memristor Switching Governed by Electrical Thresholds**, Fernando García-Redondo, Robert P. Gowers, A. Crespo-Yepes, Marisa López-Vallejo, Liudi Jiang, *IEEE Transactions on Circuits and Systems I: Regular Papers, Volume: 63, Issue: 8, Pages: 1255 - 1264. Aug. 2016. DOI: 10.1109/TCSI.2016.2564703*

2014 **Building Memristor Applications: From Device Model to Circuit Design**, Fernando García-Redondo, Marisa López-Vallejo, Pablo Ituero, *IEEE Transactions on Nanotechnology. November 2014. Volume 13, Issue 6, pp 1154-1162. DOI: 10.1109/TNANO.2014.2345093*

2012 **The tractability index of memristive circuits: branch-oriented and tree-based models**, Fernando García-Redondo, Ricardo Riaza, *Mathematical Methods in the Applied Sciences. 2012. Volume 35, Issue 14, pp 1659-1669. DOI: 10.1002/mma.2544*

Conference Papers

2019 **Applications of Computation-In-Memory Architectures based on Memristive Devices**, S. Hamdioui, H. A. Du Nguyen, M. Taouil, and A. Sebastian, M. L. Gallo, S. Pande, S. Schaafsma, F. Catthoor, S. Das, F. García-Redondo, G. Karunaratne, A. Rahimi and L. Benini, *2019 Design, Automation & Test in Europe Conference & Exhibition (DATE). 25-29 March 2019. Florence, (Italy)*

2017 **Advanced Integration of Variability and Degradation in RRAM SPICE Compact Models**, Fernando García-Redondo, Marisa López-Vallejo, *14th IEEE International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD 2017). 12 -15 June 2017. Taormina (Italy)*

2017 **CAS-T Lecture: Reconfigurable Writing Architecture for Reliable RRAM Operation in Wide Temperature Ranges**, Fernando García-Redondo, Pablo Royer, Marisa López-Vallejo, Hernán Aparicio, Pablo Ituero, Carlos A. López-Barrio, *IEEE international Symposium on Circuits and Systems, (ISCAS 2017). May 28-31 2017. Baltimore, MD, (USA)*

2017 **CAS-T Lecture: SPICE Compact Modeling of Bipolar/Unipolar Memristor Switching Governed by Electrical Thresholds**, Fernando García-Redondo, Robert P. Gowers, A. Crespo-Yepes, Marisa López-Vallejo, Liudi Jiang, *IEEE international Symposium on Circuits and Systems, (ISCAS 2017). May 28-31 2017. Baltimore, MD, (USA)*

2016 **Characterization of Analog Modules: Reliability Analyses of Radiation, Temperature and Variations Effects**, Fernando García-Redondo, Hernán Aparicio, Marisa López-Vallejo, Pablo Ituero, Carlos López-Barrio, *Conference on Design of Circuits and Integrated Systems 2016 (DCIS 2016) Granada (Spain)*

2016 **Reliable Design Methodology: The Combined Effect of Radiation, Variability and Temperature**, Fernando García-Redondo, Marisa Lopez-Vallejo, Hernán Hernán Aparicio Cerqueira, Pablo Ituero, *13 th IEEE International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD 2016). 27 - 30 June 2016. Lisbon (Portugal)*

2016 **Taxonomy of Power Supply Monitors and Integration Challenges**, Pablo Ituero, Marisa López-Vallejo, Hernán Aparicio, Fernando Garcia-Redondo, *Mixed-Signal Testing Workshop (IMSTW), 2016 IEEE 21st International. 4 - 6 July 2016. Catalonia (Spain)*

2015 **A Thermal Adaptive Scheme for Reliable Write Operation on RRAM Based Architectures**, Fernando García-Redondo, Marisa López-Vallejo, Pablo Ituero, *33rd IEEE International Conference on Computer Design, ICCD 2015, New York, (USA)*

2015 **Evolution of radiation-induced soft errors in FinFET SRAMs under process variations beyond 22nm,** Pablo Royer, Fernando García-Redondo, Marisa López-Vallejo, *Nanoscale Architectures (NANOARCH), 2015 IEEE/ACM International Symposium on. 8-10 July 2015. Boston, MA, (USA)*

2014 **A Tool for the Automatic Analysis of Single Events Effects on Electronic Circuits,** Fernando García-Redondo, Marisa López-Vallejo, Pablo Royer, Javier Agustín, *5th European Workshop on CMOS Variability, PATMOS VARI 2014. 29 September - 1 October 2014. Mallorca (Spain)*

2014 **Four-Injector Variability Modeling of FinFET Predictive Technology Models,** Pablo Royer, Marisa López-Vallejo, Fernando García-Redondo, Carlos A. López Barrio, *5th European Workshop on CMOS Variability, PATMOS VARI 2014. 29 September - 1 October 2014. Mallorca (Spain)*

2013 **Improvement of Radar Capabilities by Reconfigurable Digital Signal Processing,** Fernando García-Redondo, Víctor Iglesias, Miguel A. Sánchez, Jesús Grajal, Marisa López-Vallejo, Carlos López-Barrio, *Conference on Design of Circuits and Integrated Systems 2013 (DCIS 2013) San Sebastián (Spain)*

2012 **Model Validation and Simulation Framework for Novel Nanometer Devices,** Fernando García-Redondo, Marisa López-Vallejo, Pablo Ituero, Carlos López Barrio, *Conference on Design of Circuits and Integrated Systems 2012 (DCIS 2012). 28-30 November 2012. Avignon (France)*

2012 **A CAD Framework for the Characterization and Use of Memristor Models,** Fernando García, Marisa López-Vallejo, and Pablo Ituero, *International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design 2012 (SMACD2012). 19 - 21 September 2012. Seville (Spain)*

2012 **Temperature Sensor Placement Including Routing Overhead and Sampling Inaccuracies,** Pablo Ituero, Fernando García, and Marisa López-Vallejo, *International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design 2012 (SMACD2012). 19 - 21 September 2012. Seville (Spain)*

2011 **Assessing Self-Learning Electronics Through the Support of Remote Labs,** Marisa López-Vallejo, Pablo Ituero, Ángel Férnandez-Herrero, and Fernando García, *IADIS International Conference on e-Learning 2011 (EL 2011). 20 - 23 July 2011. Rome, Italy*

2010 **Web-based Integrated Environment for Self-learning Electronics: the Analog and Digital Laboratory at Home,** Ángel Fernández-Herrero, Pablo Ituero, Marisa López-Vallejo, Fernando García Redondo, *Interactive Computer Aided Learning (ICL 2010), 15-17 September 2010. Hasselt (Belgium)*

PhD. Thesis

June 2017 **Resistive RAM: Simulation and Modeling for Reliable Design,** Fernando García Redondo, *Advised by Marisa López-Vallejo. DOI: 10.20868/UPM.thesis.46845. Department of Electronic Engineering. Universidad Politécnica of Madrid*

Master Thesis

Feb. 2012 **Design and Implementation of a Simulation Framework for Circuits Using Memristors,** Fernando García Redondo, *Dept. Electronic Engineering and Dept. Applied Mathematics for Information Technology. Universidad Politécnica de Madrid*

Research Projects

March. 2018 - Now **(EU H2020: No 780215) MNEMOSENE, "Computation-In-Memory Architectur based on Resistive Devices",** Main Researcher: Prof. Said Hamdioui. Financing Entity: European Union's Horizon 2020. Participants: TU Delft, TU Eindhoven, RWTH Aachen, ETH Zurich, IBM Research GmbH, Arm Ltd., INRIA, Imec, Intelligentsia Consultants

Jan. 2016 - Dec. 2018 **(TEC2012-31292) TOLERA 2, "PVT-Variations and radiation tolerance in nanometric technologies",** Main Researcher: María Luisa López Vallejo. Financing Entity: CICYT Spanish Ministry of Economy and Competitiveness. Participants: Integrated Systems Laboratory, UPM, (6 researchers)

Sept. 2015 - May. 2017 **(Ref. E9364) EUROSTARS LIBRA, "Support for the definition, design, development and validation of a library standard radiation-hardened cell microelectronics, compatible with IHP technology SGB25RH",** UPM Main Researcher: María Luisa López Vallejo. Financing Entity: European Commission-7th Framework Programme. Participants: Arquimea, IHP, Silicon Radar Gmbh, UPM, (19 researchers)

Dec. 2014 - Nov. 2016 **(TEC2014-53909-REDT) "NANOVAR, Thematic network on nanoelectronics variability",** Main Researcher: Montserrat Nafría. Financing Entity: CICYT Spanish Ministry of Economy and Competitiveness. Participants: 8 Spanish Research Entities, (135 researchers)

Jan. 2013 - Dec. 2015 **(TEC2012-31292) TOLERA, "PVT-Variations and radiation tolerance in nanometric technologies",** Main Researcher: María Luisa López Vallejo. Financing Entity: CICYT Spanish Ministry of Economy and Competitiveness. Participants: Integrated Systems Laboratory, UPM, (6 researchers)

Jan. 2013 - Dec. 2014 **(IPT-2012-0422-370000) RAD-HARQ "Development of technology hardened against radiation for space microelectronics",** UPM Main Researcher: María Luisa López Vallejo. Financing Entity: CICYT Spanish Ministry of Economy and Competitiveness. Participants: Arquimea and Integrated Systems Laboratory, UPM, (12 researchers)

Jan. 2011 - Oct. 2014 **(TEC2011-15599-E) VARIABLES, "Spanish Network: variability in micro/nanoelectronic technologies, circuits and systems",** Main Researcher: Montserrat Nafría. Financing Entity: CICYT Spanish Ministry of Economy and Competitiveness. Participants: 11 Spanish Research Entities, (168 researchers)

May. 2011 - Apr. 2013 **(FP7-SEC-2010-1) BASYLIS, "Mobile, Autonomous and affordable system to increase safety in large unpredictable environments",** Main Researcher: Jesús Grajal – Francisco Segura Financing Entity: European Commission-7th Framework Programme. Participants: Indra S.A. (Spain), NTGS (Spain),University of Florence, Terma (Den.),Microflown Technologies (Neth.), Mirasys (Fin.), UPM (Spain), University College London (UK), NCPCI (Spain), (6 UPM researchers)

Nov. 2012 - Dec. 2014 **(TSI-020601-2012-21) AMISTAD, "Intelligent multifunctional antennas compatible with SDR with advanced digital TTD technology",** Main Researcher: Félix Pérez Martínez Financing Entity: Spanish Ministry of Industry, Energy and Tourism Participants: Indra S.A., UPM

Jan. 2011 - Dec. 2013 **(MTM2010-1512) MICINN "Algebraic-differential systems: analysis, diagnosis of failures and applications in electrical and electronic engineering",** Collaborating as student. Main Researcher: Ricardo Riaza Rodríguez. Financing Entity: Spanish Ministry of Science and Innovation. Participants: Group of Dynamic Systems, Learning and Control (SISDAC), UPM, (6 researchers)

Jan. 2011 - Dec. 2011 **(CCG10-UPM/ESP-5236) "Methods of automatic generation of circuital models: analytical and computational aspects",** Collaborating as student. Main Researcher: Ricardo Riaza Rodríguez. Financing Entity: Comunidad de Madrid, Spain. Participants: Group of Dynamic Systems, Learning and Control (SISDAC), UPM, (7 researchers)

Jan. 2010 - Dec. 2012 **(TEC2009-08589) Delta "Advanced electronic design: power, temperature and high performance",** Main Researcher: María Luisa López Vallejo. Financing Entity: CICYT Spanish Ministry of Economy and Competitiveness. Participants: Integrated Systems Laboratory, UPM, (6 researchers)

Innovation Projects

Sept. 2008 - Aug. 2009 **"Extension of the hardware simulation laboratory through the elaboration of a library of examples and the incorporation of remote access",** Main Researcher: María Luisa López Vallejo. Financing Entity: UPM. Participants: Educational Innovation Group of the Electronic Engineering Department, UPM, (12 researchers)

Sept. 2007 - Aug. 2008 **"24 hour remote access to real prototype platforms in teaching laboratories of hardware design",** Main Researcher: Ángel Fernández Herrero Financing Entity: UPM. Participants: Educational Innovation Group of the Electronic Engineering Department, UPM, (10 researchers)